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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/822,532	03/30/2001	Cheng-Wei Lee	67,200-390	4786

7590 04/17/2003

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EXAMINER
KUNEMUND, ROBERT M

ART UNIT	PAPER NUMBER
1765	4

DATE MAILED: 04/17/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/822,532	LEE, CHENG-WEI	
	Examiner	Art Unit	
	Robert M Kunemund	1765	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 January 2003* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

The Rejection

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1 to 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chakravorty (US 6,181,569) in view of Lin (US 6,383,916) and further in view of Wolf et al., "Silicon Processing for the VLSI Era", vol. 1, page 529.

Chakravorty discloses a low cost chip size package and method of fabricating the same. A wafer is provided which contains numerous integrated circuit chips. The wafer contains input and output contact pad regions, referred to as chip contact pads (Column 7, lines 45-55). This reads on the applicant's limitation of providing a pre-processed electronic electronic substrate with a plurality of input/output pads formed on a top surface. A dielectric layer is deposited on a wafer. The dielectric layer can be a photosensitive material such as polyimide. Clearance holes are formed in the wafer. The clearance holes could be fabricated by well known lithographic techniques. Clearance holes are made by etching the film selectively over the I/O pad regions by using a mark. This reads on the applicant's limitation of photolithographically forming a plurality of openings with one on each of the plurality of I/O pads. Next, a metal layer is

deposited which electrically connects to the chip contact pads. The metal layer could be aluminum, chromium, nickel or a combination of metal or multiple metal layers. The metal is deposited using established techniques such as sputtering (Column 8, lines 32-45). This reads on the applicant's limitation of sputter depositing a metal comprising Al filling said plurality of opening and covering a top surface of the insulating material layer. Metal bump regions are formed in the structure. Methodologies established in the area of chemical-mechanical polishing could also be employed for a controlled processes for exposure of the metal bump regions. The layers not covered by bumps are removed by an etching process.

Unlike the claimed invention, Chakravorty does not teach a method for removing the insulating material by a wet etching process.

Lin teaches a method of closely interconnecting integrated circuits contained within a semiconductor wafer to electrical circuits surrounding the semiconductor wafer. A silicon wafer is provided. A dielectric layer is deposited over the devices and the substrate. A thick polyimide layer is deposited over the substrate. The polyimide layer is etched under an angle of about 75 degrees with the following curing being done under and angle of 45 degrees. When a photosensitive polymer is used, a wet etch can be applied (Column 7, lines 42-60).

It is the Examiner's position that a person having ordinary skill in the art would have found it obvious to modify Chakravorty with method of wet etching the polyimide material, the insulating material, as taught by Lin. Chakravorty is not particular about the type of etching process used to remove the insulating material and since wet etching is a known process that has found widespread acceptance in microelectronic fabrication (See Silicon Processing for the VLSI Era, Volume 1, page 529) its use would have been anticipated in order to achieve a reasonable expectation of success.

Response to Applicant's Arguments

Applicant's arguments filed January 21, 2003 have been fully considered but they are not persuasive.

Applicants' argument concerning the thickness of the insulating material is noted. However, the Lin reference does teach that the insulating layer be about the same thickness of the bump. Also, the reference clearly, shows a polyimide layer thicker then 5μm as claimed.

Applicant's argument concerning the partial removal of the insulating material has been considered and not deemed persuasive. The Chakravorty reference does teach col. 11, that by using an etch method to control exposure at the bumps, which includes thinning the insulation material as claimed. Also, note figures.

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication should be directed to Robert Kunemund at telephone number (703) 308-1091.

R. Kunemund/mn
April 8, 2003

ROBERT KUNEMUND
PRIMARY EXAMINER